UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,466	06/29/2001	Ajit V. Sathe	219.40241X00	5280

7590 10/20/2004

MICHAEL D PLIMIER
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,466	SATHE, AJIT V.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-39 and 46-64* is/are pending in the application.

4a) Of the above claim(s) *19,24-26,32,37-39,50,57 and 62-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-18,20-23,27-31,33-36,46-49,51-56 and 58-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 2, 2004 have been fully considered. The argument with respect to claim rejection under 35 USC 112, for claims 14-18, 20-23, 27-31, 33-36, 46-49, 51-56 and 58-61 are not persuasive, except 112 second paragraph rejection regarding claims 52-56 and 58-61, for the input/out put device. Applicant argues that the definition cited by the examiner based on the IEEE standard is the correct definition. However, that definition was used as a plain meaning of the word, which will be a base for applying a prior art. Applicant's disclosure has failed to defined / describe the terms "thin core" and "coreless", to reasonable convey to one skilled in the relevant art. Applicant point out to a document, a publication by Kevin Teixeira of Intel Corporation, titled "Bumpless Build-Up layer Packaging Technology", submitted by the applicant as an example and for teaching purpose. However, that document is just another example and does not define the "thin core" and "coreless" substrate. Applicant further argues that any layer on which other layers are formed is not the central layer or basic support. Without pointing out a support in the specification, the applicant is arguing on the definition given by the examiner and not clarifying why any layer cannot be considered as a basic support layer or core layer. The core layer or basic support may have other layers on only one side of the core layer or basic support layer, or may have different number of layers on opposite side of the core layer or basic support layer. Examiner respectfully disagrees and rejection is maintained.

112 second paragraph rejection regarding claims 52-56 and 58-61, for the input/out put device has been withdrawn herewith, in view of the clarification made in the response of August 2, 2004.

2. Applicant's arguments relating to the art rejection with respect to claims 14-18, 20-23, 27-31, 33-36, 46-49 and 51 have been considered but are moot in view of the new ground(s) of rejection, this new ground being necessitated by amendment.

Claim Objections

3. Claims 46-49 and 51 are objected to because of the following:

Regarding claim 46, "a stiffener secured onto the **at least one of a coreless substrate**", line 5, is misguiding. If "**a coreless substrate**" is referring to the coreless substrate as stated in line 2, it should be changed to **the coreless substrate**.

Claims 47-49 and 51 depend upon claim 46 and inherit the same deficiency.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 14-18, 20-23, 27-31, 33-36, 46-49, 51-56 and 58-61 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description

requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

"Thin core" or "coreless" substrate is explained in the disclosure by a working example. However, "core" as defined in The IEEE Standard Dictionary of Electronic and Electronics Terms, Sixth Edition, is the central layer or basic support of **certain types of laminated media**. For a person of ordinary skill in the art, a core layer in the substrate will be any layer on which other layers are formed. The core layer may be located in the center of the substrate or at any other location in the substrate.

In the specification there is no explanation of what is a "core". There is only example of layer, which meets the definition above. The example identifies the thickness for the core layer as 0.1 to .5 mm, and more specifically about 0.4 mm. However, it is not clear, whether, all the layers are having the thickness as described, less than 0.5 mm, or there may be a presence of a layer with a thickness more than 0.5 mm. Also, if all the layers are with the thickness of 0.5 mm or less, why couldn't any of the layers be a core layer, and that makes the concept of the coreless substrate unclear. It is unclear for a person of ordinary skill in the art to understand what constitute a thin core or coreless substrate according to the specification and what is the difference between the coreless and thin core substrate.

Claims 14-18, 20-23, 27-31, 33-36, 46-49, 51-56 and 58-61 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. "Thin core" or "coreless" substrate is explained in the disclosure by a working example. However, "core" as defined in The IEEE Standard Dictionary of Electronic and Electronics Terms, Sixth Edition, is the central layer or basic support of certain types of laminated media. For a person of ordinary skill in the art, a core layer in the substrate will be any layer on which other layers are formed. The core layer may be located in the center of the substrate or at any other location in the substrate.

In the specification there is no explanation of what is a "core". There is only example of layer, which meets the definition above. The example identifies the thickness for the core layer as 0.1 to .5 mm, and more specifically about 0.4 mm. However, it is not clear, whether, all the layers are having the thickness as described, less than 0.5 mm, or there may be a presence of a layer with a thickness more than 0.5 mm. Also, if all the layers are with the thickness of 0.5 mm or less, why couldn't any of the layers be a core layer, and that makes the concept of the coreless substrate unclear. It is unclear for a person of ordinary skill in the art to understand what constitute a thin core or coreless substrate according to the specification and what is the difference between the coreless and thin core substrate.

Therefore, for the examination purpose, the examiner assumes the coreless / thin core substrate is a substrate with each of the layers constituting the substrate having a thickness not more than 0.5 mm, excluding the stiffener.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 14-18, 20-23, 27-31, 33-36, 46-49, 51-56 and 58-61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In all of the above claims the applicant is claiming a stiffener to provide stiffening to one of a "thin core and coreless substrate". It is not clear to the examiner as to what is meant by a "thin core and coreless substrate".

"Thin core" or "coreless" substrate is explained in the disclosure by a working example. However, "core" as defined in The IEEE Standard Dictionary of Electronic and Electronics Terms, Sixth Edition, is the central layer or basic support of certain types of laminated media. For a person of ordinary skill in the art, a core layer in the substrate will be any layer on which other layers are formed. The core layer may be located in the center of the substrate or at any other location in the substrate.

In the specification there is no explanation of what is a "core". There is only example of layer, which meets the definition above. The example identifies the thickness for the core layer as 0.1 to .5 mm, and more specifically about 0.4 mm. However, it is not clear, whether, all the layers are having the thickness as described,

less than 0.5 mm, or there may be a presence of a layer with a thickness more than 0.5 mm. Also, if all the layers are with the thickness of 0.5 mm or less, why couldn't any of the layers be a core layer, and that makes the concept of the coreless substrate unclear. It is unclear for a person of ordinary skill in the art to understand what constitute a thin core or coreless substrate according to the specification and what is the difference between the coreless and thin core substrate.

Therefore, for the examination purpose, the examiner assumes the coreless / thin core substrate is a substrate with each of the layers constituting the substrate having a thickness not more than 0.5 mm, excluding the stiffener.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 14-18, 20-23, 27-31, 33-36, 46-49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al., US Patent No. 6,020,221, in view of Yamashita et al., US Patent No. 5,777,387, Murasawa, US Patent 5,841,188, Honda, US Patent No. 6,406,942 and Ho, US Patent No. 6,221,693.

Regarding claim 14, Lim et al. discloses an integrated circuit printed circuit board (IC-PCB) carrier package having substrate (element 14, figure 2-8), and

a stiffener (element 20, figure 2-8) to provide stiffening support to the substrate (column 4, line 40-50).

Lim et al., does not state that the substrate is thin core or coreless substrate but in view of the explanation in the 112 rejections, examiner notes that Lim et al.'s structure can be reasonably construed to be thin core or coreless because Lim et al., discloses the substrate can be PTFE (Teflon) or Polyamide Tape, column 5, line 59-60 and the structure can be a thin film structure, column 5, line 65. Therefore, the construction of Lim et al., teaches thin core or coreless substrate.

Lim et al., fails to explicitly disclose the substrate includes at least five layers, none of the layers having a thickness of greater that about 0.5mm. However, Lim et al., discloses that substrate structure can be made of other known substrate material such as PTFE (Teflon), polyamide tape, BT-FR4 and BT-FR5, column 5, line 55-60, and in a thin film single layer construction, column 5, line 64-67 and further discloses that substrate construction varies from thin film single layers to complex thick film multiplayer versions, column 5, line 64-67, thereby implying that all known constructions of single film and multiplayer films, thick or thin, are contemplated.

Further, Ho teaches that multiplayer, 5 layers, thin layer substrates are known and old. Further, Ho teaches that use of 10-40 micron thickness for those layers is also known (five dielectric layers, each with a thickness of about 10 to 40 micrometer, column 4, line 41-53 and four thin film metal layers, figure 4).

Further evidence that thin film multiplayer, 5 layers, substrates are known in the art is given by Honda, (element 9, figure 3N, five dielectric layers, four conductive layers) with very low pitch pattern.

Further evidence of the substrates that are having very thin layers in the micron ranges and are known in the art is given by Yamashita and Murasawa.

Yamashita et al., in the background disclosure discloses that polyimide is generally used as the base material with a tape thickness of about 50-125 μm, in a BGA package film carrier with a stiffener to avoid warping and waviness, column 2, line 39-46.

Murasawa discloses a tape carrier with a preferable thickness of polyimide tape 3 less than or equal to 50 μm.

Yamashita and Murasawa discloses that it is well known in the art to use a tape with thickness of 50-125 μm or less than 50 μm as a single film substrate, Ho discloses that it is well known in the art to use thin film multiplayer substrate with a film thickness of between 10-40 microns and Honda discloses that it is well known in the art to use thin film multiplayer substrate, for a semiconductor package.

Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide the package of Lim et al., with multilayer thin film substrate having five layers and none of the layers with a thickness of greater than

about 0.5 mm (500 micron), as taught by Ho, in order to have a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device with very low pattern pitch, as evinced by Yamashita et al., Murasawa and Honda, because it is well known and further suggested by Lim et al.

Regarding claim 27, Lim et al., discloses a packaged integrated circuit (1C) comprising:

an IC (element 12, figure 2-8), and

an integrated circuit printed circuit board (IC-PCB) carrier package having a substrate (element 14, figure 2-8), and a stiffener (element 20, figure 2-8) to provide stiffening support to the substrate (column 4, line 40-50).

Lim et al., does not state that the substrate is thin core or coreless substrate but in view of the explanation in the 112 rejections, examiner notes that Lim et al.'s structure can be reasonably construed to be thin core or coreless because Lim et al., discloses the substrate can be PTFE (Teflon) or Polyamide Tape, column 5, line 59-60 and the structure can be a thin film structure, column 5, line 65. Therefore, the construction of Lim et al., teaches thin core or coreless substrate.

Lim et al., fails to explicitly disclose the substrate includes at least five layers. However, Lim et al., discloses that substrate structure can be made of other known substrate material such as PTFE (Teflon), polyamide tape, BT-FR4 and BT-FR5, column 5, line 55-60, and in a thin film single layer construction, column 5, line 64-67

and further discloses that substrate construction varies from thin film single layers to complex thick film multiplayer versions, column 5, line 64-67, thereby implying that all known constructions of single film and multiplayer films, thick or thin, are contemplated.

Further, Ho teaches that multiplayer, 5 layers, thin layer substrates are known and old. Further, Ho teaches that use of 10-40 micron thickness for those layers is also known (five dielectric layers, each with a thickness of about 10 to 40 micrometer, column 4, line 41-53 and four thin film metal layers, figure 4).

Further evidence that thin film multiplayer, 5 layers, substrates are known in the art is given by Honda, (element 9, figure 3N, five dielectric layers, four conductive layers) with very low pitch pattern.

Further evidence of the substrates that are having very thin layers in the micron ranges and are known in the art is given by Yamashita and Murasawa.

Yamashita et al., in the background disclosure discloses that polyimide is generally used as the base material with a tape thickness of about 50-125 μm, in a BGA package film carrier with a stiffener to avoid warping and waviness, column 2, line 39-46.

Murasawa discloses a tape carrier with a preferable thickness of polyimide tape 3 less than or equal to 50 μm.

Yamashita and Murasawa discloses that it is well known in the art to use a tape with thickness of 50-125 μm or less than 50 μm as a single film substrate, Ho discloses that it is well known in the art to use thin film multiplayer substrate with a film thickness

of between 10-40 microns and Honda discloses that it is well known in the art to use thin film multiplayer substrate, for a semiconductor package.

Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide the package of Lim et al., with multilayer thin film substrate having five layers, as taught by Ho, in order to have a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device with very low pattern pitch, as evinced by Yamashita et al., Murasawa and Honda, because it is well known and further suggested by Lim et al.

Regarding claim 46, Lim et al., discloses an integrated circuit printed circuit board (IC-PCB) carrier package having a substrate (element 14, figure 2-8), and

a stiffener (element 20, figure 2-8) secured onto the substrate of the integrated circuit printed circuit board (IC-PCB) carrier package to provide stiffening support thereto (column 4, line 40-50).

Lim et al., does not state that the substrate is thin core or coreless substrate but in view of the explanation in the 112 rejections, examiner notes that Lim et al.'s structure can be reasonably construed to be thin core or coreless because Lim et al., discloses the substrate can be PTFE (Teflon) or Polyamide Tape, column 5, line 59-60

and the structure can be a thin film structure, column 5, line 65. Therefore, the construction of Lim et al., teaches thin core or coreless substrate.

Lim et al., fails to explicitly disclose the substrate includes at least five layers, none of the layers having a thickness of greater that about 30 microns. However, Lim et al., discloses that substrate structure can be made of other known substrate material such as PTFE (Teflon), polyamide tape, BT-FR4 and BT-FR5, column 5, line 55-60, and in a thin film single layer construction, column 5, line 64-67 and further discloses that substrate construction varies from thin film single layers to complex thick film multiplayer versions, column 5, line 64-67, thereby implying that all known constructions of single film and multiplayer films, thick or thin, are contemplated.

Further, Ho teaches that multiplayer, 5 layers, thin layer substrates are known and old. Further, Ho teaches that use of 10-40 micron thickness for those layers is also known (five dielectric layers, each with a thickness of about 10 to 40 micrometer, column 4, line 41-53 and four thin film metal layers, figure 4).

Further evidence that thin film multiplayer, 5 layers, substrates are known in the art is given by Honda, (element 9, figure 3N, five dielectric layers, four conductive layers) with very low pitch pattern.

Further evidence of the substrates that are having very thin layers in the micron ranges and are known in the art is given by Yamashita and Murasawa.

Yamashita et al., in the background disclosure discloses that polyimide is generally used as the base material with a tape thickness of about 50-125 μm, in a BGA

package film carrier with a stiffener to avoid warping and waviness, column 2, line 39-46.

Murasawa discloses a tape carrier with a preferable thickness of polyimide tape 3 less than or equal to 50 μm.

Yamashita and Murasawa discloses that it is well known in the art to use a tape with thickness of 50-125 μm or less than 50 μm as a single film substrate, Ho discloses that it is well known in the art to use thin film multiplayer substrate with a film thickness of between 10-40 microns and Honda discloses that it is well known in the art to use thin film multiplayer substrate, for a semiconductor package.

Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide the package of Lim et al., with multilayer thin film substrate having five layers and none of the layers with a thickness of greater than about 30 micron, as taught by Ho, in order to have a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device with very low pattern pitch, as evinced by Yamashita et al., Murasawa and Honda, because it is well known and further suggested by Lim et al.

Regarding claims15, 28 and 47, the modified assembly of Lim et al., further discloses flip chip ball grid array carrier package (see figure 8, column 3, line 57-60).

Regarding claims16, 29 and 48, the modified assembly of Lim et al., further discloses the stiffener member made of ceramic material (claims 16 and 48, column 5, line 18-24) or thermosetting plastic material (claim 29, column 3, line 1-20, polyphenylene sulfide, which is polymer and has a thermosetting property).

Regarding claims 17, 30 and 49, the modified assembly of Lim et al., further discloses the stiffener being planar for mounting to a die-side major planar surface of the substrate (see figure 8).

Regarding claims18 and 31, the modified assembly of Lim et al., further discloses an internal window in the stiffener (see figure 8).

Regarding claims 20 and 33, the modified assembly of Lim et al., further discloses the above substrate height of the stiffener equal to that of the above substrate height of the semiconductor chip (see figure 8).

Regarding claims 23 and 36, the modified assembly of Lim further discloses stiffener made of copper, which is conductive with an epoxy resin layer in-between (column 4, line 40-50, see figure 8).

10. Claims 21, 22, 34, 35 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Lim et al., US Patent No. 6,020,221, Yamashita et al., US Patent No. 5,777,387, Murasawa, US Patent 5,841,188, Honda, US Patent No. 6,406,942 and Ho, US Patent No. 6,221,693, as applied to claims 14, 27 and 46 above, and further in view of Uchida et al., US Patent No. 5,391,924 and Glen, US Patent No. 6,150,193.

Regarding claims 21 and 34, the applicant is further claiming the stiffener having a top surface above a substrate plane, which is substantially co-planar with, when mounted, a top surface of a combination of an IC die with an integrated heat spreader.

The modified structure of Lim et al., discloses all the features of the claimed invention as applied to claims 14 and 27 above, including the stiffener having a top surface above a substrate plane, which is substantially co-planar with, when mounted, a top surface of a semiconductor device (element 12, figure 8, of Lim et al.,) but fails to explicitly disclose the device has an IC die with an integrated heat spreader.

Glenn discloses a package wherein the encapsulating materials with inorganic filler 42 and a heat slug 43 to work as heat spreader, figure 1 and 11, column 10, line 1-15, to dissipate heat to outside environment.

Uchida et al., discloses a semiconductor device wherein the semiconductor element is encapsulated with an epoxy resin composition exhibiting a high heat conductivity, column 2, line 1-15.

As disclosed by Glenn and Uchida et al., the semiconductor package, encapsulated in a heat conductive resin as an integral part of the package, is known in the art for dissipating the heat to the environment.

Therefore, it would have been obvious to a person of ordinary skill in the art to construe the semiconductor package of Lim et al., with an IC die having integrated heat spreader, as disclosed by Glenn and Uchida et al., in order to dissipate heat to the environment, and therefore meet the limitation.

Regarding claim 22, 35 and 51, the modified assembly of Lim et al., further discloses, the stiffener can co-support a heat sink as shown in figure 8.

Allowable Subject Matter

11. Claims 52-61 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, Ist and 2nd paragraph, set forth in this Office action.

12. The following is a statement of reasons for the indication of allowable subject matter: The prior art, though disclose a thin film multilayer substrate, does not disclose or suggest the specific substrate that includes a thin-core with a thickness between about 0.1 mm and 0.5 mm and at least four laminate layers, at least two of the laminate layers on a first side of the thin core and at least two of the laminate layers on a second side of the thin core, none of the laminate layers having a thickness greater than about 30 microns, together with other claim limitations.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

I B Patel
Examiner
Art Unit: 2841
October 9, 2004

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800